ELEC50001 – Circuits and Systems

2021 - 2022

Answer ALL questions.

There are THREE questions on the paper.

Question ONE counts for 50% of the marks, other questions 25% each

Time allowed: 2 hours

Information for Candidates:

The following notation is used in this paper:

1. Unless explicitly indicated otherwise, digital circuits are drawn with their inputs on the left and their outputs on the right.
2. Within a circuit, signals with the same name are connected together even if no connection is shown explicitly.
3. The notation X[2:0] denotes the three-bit number X2, X1 and X0. The least significant bit of a binary number is always designated bit 0.

1. (a) Part of the datasheet for AD823, a dual operational amplifier integrated circuit, is provided as a separate document for your convenience.

Based on the information available, answer the following questions with appropriate justifications.

(i) *Figure 1.1(a)* shows half of the AD823 connected as an amplifier. Sketch the output signal V_{OUT} if the input signal V_{IN} is a sinewave at 3.2MHz with an amplitude of 0.1V and a DC offset of 0.2V. State any assumptions made.

[4]

(ii) Sketch the output signal V_{OUT} if the input signal V_{IN} is a symmetrical digital clock signal at a frequency of 1MHz with low and high logic levels at 0V and 0.3V.

[3]

(iii) *Figure 1.1(b)* shows the AD823 connected as audio amplifier for input signal in the frequency range of 20Hz to 20kHz driving a 32Ω headphone.

I. What is the gain of the amplifier at the specified frequency range?
II. What is the DC operating voltage at nodes A, B and C?
III. What value would you choose for the value of R in *Figure 1.1(b)* and why?
IV. What is a suitable value of the output capacitor C_{OUT} and why?

[5]

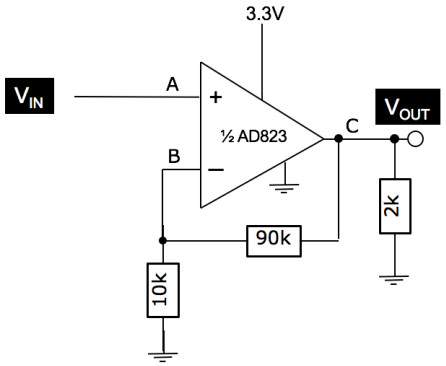

Figure 1.1(a)

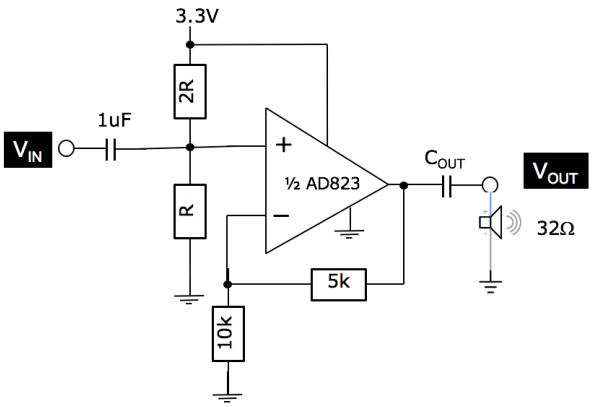

Figure 1.1(b)

(b) A 16-bit microprocessor system has 32k byte of RAM, 8k byte of ROM and two I/O devices each occupy 4 bytes of the memory address space. The microprocessor has a 16-bit address bus A[15:0]. The starting addresses of the RAM, ROM and I/O devices are shown in *Figure 1.2*.

(i) What is the address range of each of the devices?

[4]

(ii) Design in the form of Boolean equations the chip select signals RAM_CS, ROM_CS, IO1_CS and IO2_CS. You may assume that the chip select signals are low-active in all cases.

[4]

(iii) Implement in Verilog this address decoder module.

[2]

Device	Starting Address (in Hex)
RAM	0000
ROM	A000
I/O 1	FE00
I/O 2	FF00

Figure 1.2

(c) *Figure 1.3* shows a circuit with two D flip-flops FF1 and FF2 with setup and hold times of 2 ns and 1 ns respectively, and a clock-to-Q output delay of 1 ns. The clock signal CLK has a 1:1 mark-space ratio. The signal path has two combinational circuits, LUT_1 and LUT_2, each having a propagation delay between 1 ns and 5 ns. The clock path is driven by non-inverting clock buffer, which has a propagation delay between 2 ns and 10 ns.

(i) Derive the inequalities for the setup time constraints for this circuit.

[4]

(ii) Hence derive the maximum frequency of the signal CLK for reliable operation of this circuit.

[2]

(iii) How would you modify the circuit to increase the maximum operating clock frequency? What is the new maximum frequency?

[4]

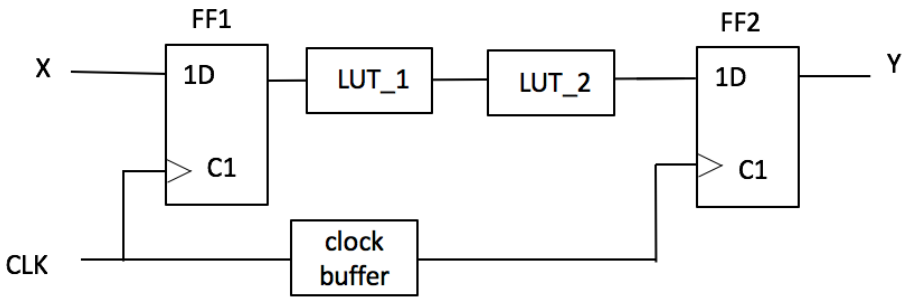

Figure 1.3

(d) You are required to convert a 10-bit digital number to an analogue voltage over the voltage range of 0 to 3.3V with a Digital-to-Analogue Converter (DAC).

(i) What is the resolution of the analogue output?

[2]

(ii) *Figure 1.4* shows the circuit of a 4-bit DAC using R-2R ladder architecture, four electronic switches and a current summing operational amplifier. Derive the value I_o flowing through the bottom 2R resistor (in terms of R). Hence or otherwise, derive the value of I_{in}, the input current from the voltage reference V_{ref}. What is the output voltage V_{out} of the DAC with the switch setting as shown in *Figure 1.4*?

[6]

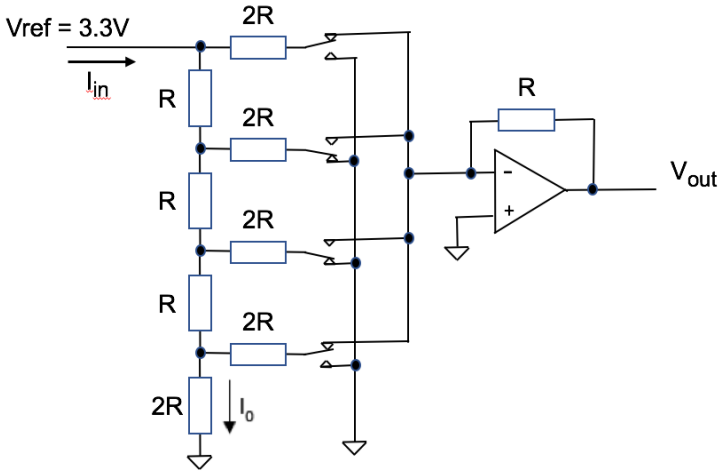

Figure 1.4

(e) A circuit with a 4-bit unsigned input X[3:0] and a 4-bit unsigned output Y[3:0] is required to perform a decoding function as described by the following pseudo-code:

```
if X < 5
      Y = X
else if  X < 12
      Y = X + 3
else
      Y = X – 2
```

(i) Design this decoder circuit in Verilog HDL with the interface declarations shown in *Figure 1.5* using the CASE statement.

[8]

(ii) If the decoder is implemented using Intel's MAX-10 FPGA, estimate the number of Logic Elements (LEs) required.

[2]

```
module decoder (X, Y);
   input    [3:0] X;
   output   [3:0] Y;
```

Figure 1.5

2. (a) *Figure 2.1* shows an integrator circuit implemented using a dual supply operational amplifier. Derive from first principle the relationship between V_{OUT} and V_{IN}, and hence shows that the transfer function of this circuit is:

$$K(s) = \frac{V_{out}(s)}{V_{in}(s)} = -\frac{1}{RC} \times \frac{1}{s}$$

[5]

(b) *Figure 2.2* shows a summing integrator with two input voltages X and Y. Shows that the relationship between the output V_1 and the inputs X and Y is given by the following:

$$V_1(s) = -\frac{1}{\frac{1}{2} + 10RCs}\,(X(s) + Y(s))$$

[10]

(c) *Figure 2.3* shows a filter circuit combining the circuits from (a) and (b) above and feedback. Show that the transfer function of this circuit is that of a second-order low pass filter of the form:

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = -\frac{1000}{s^2 + 5s + 1000}$$

[10]

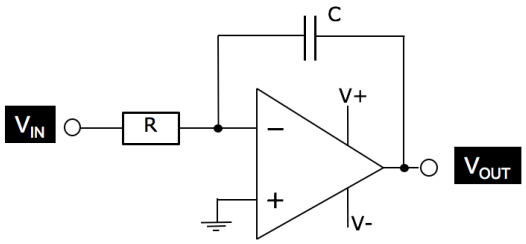

Figure 2.1

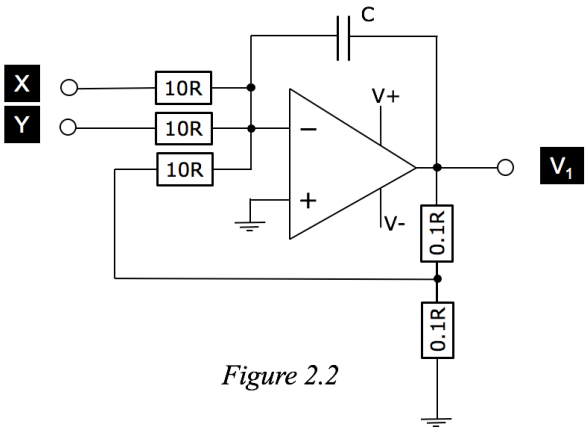

Figure 2.2

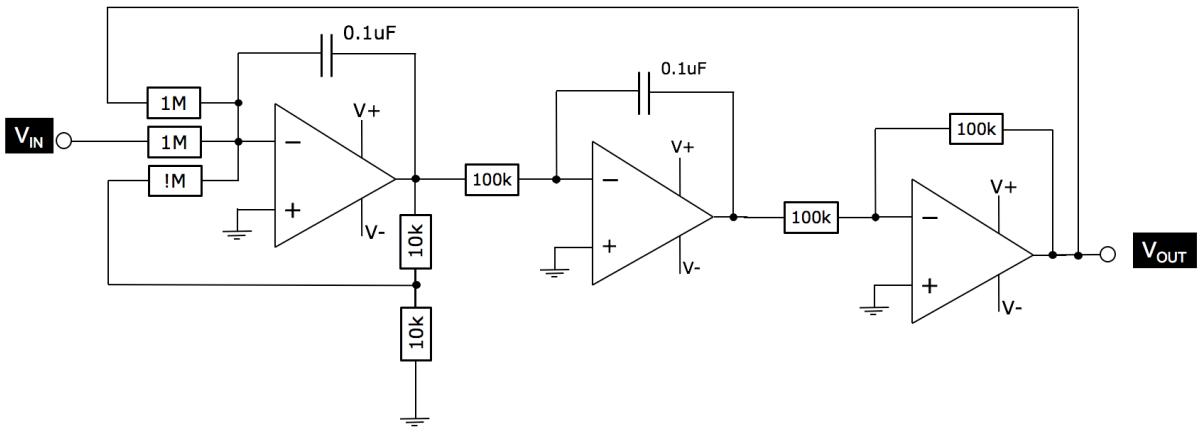

Figure 2.3

3. *Figure 3.1* shows the top-level schematic of the serial peripheral interface SPI used to interface between the MAX10 FPGA board and a digital to analogue converter.

a) Specify in Verilog HDL the divide-by-50 clock circuit that produces the 1MHz internal symmetrical clock signal clk_1MHz (i.e. 1:1 mark-space ratio) from the 50MHz system clock.

[5]

b) *Figure 3.2* shows the state diagram of the "load detector" FSM circuit. Specify in Verilog HDL the code segment that implements this FSM.

[10]

c) *Figure 3.3* shows the code segment of the 16-bit data shift register circuit in Verilog HDL. Draw the digital circuit that is expected to be synthesized, using only D flip-flops, multiplexers and basic logic gates.

[10]

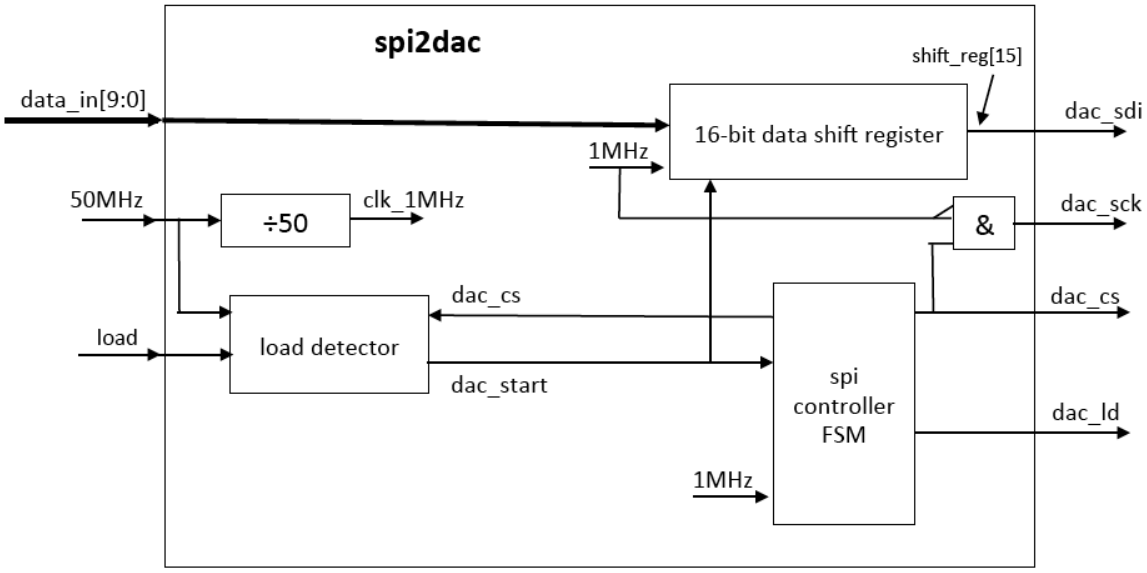

Figure 3.1

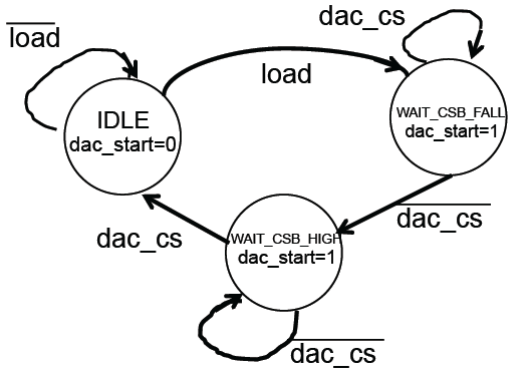

Figure 3.2

```
input [9:0] data_in; // input data to DAC
wire [9:0]  data_in;
reg         dac_cs, dac_ld;
wire        dac_sck, dac_sdi;

parameter   BUF=1'b1;      // 0:no buffer, 1:Vref buffered
parameter   GA_N=1'b0;     // 0:gain = 2x, 1:gain = 1x
parameter   SHDN_N=1'b1;   // 0:power down, 1:dac active

wire [3:0] cmd = {1'b0,BUF,GA_N,SHDN_N};  // wire to VDD or GND

// shift register for output data
reg [15:0] shift_reg;
initial  begin
   shift_reg = 16'b0;
   end

always @(posedge clk_1MHz)
   if((dac_start==1'b1)&&(dac_cs==1'b1))     // parallel load data to shift reg
      shift_reg <= {cmd,data_in,2'b00};
   else                                      // .. else start shifting
      shift_reg <= {shift_reg[14:0],1'b0};

// Assign outputs to drive SPI interface to DAC
      assign dac_sck = !clk_1MHz&!dac_cs;
      assign dac_sdi = shift_reg[15];
```

Figure 3.3

ANALOG DEVICES

Dual, 16 MHz, Rail-to-Rail FET Input Amplifier

Data Sheet **AD823**

FEATURES

- Single-supply operation
  - Output swings rail-to-rail
  - Input voltage range extends below ground
  - Single-supply capability from 3 V to 36 V
- High load drive
  - Capacitive load drive of 500 pF, G = +1
  - Output current of 15 mA, 0.5 V from supplies
- Excellent ac performance on 2.6 mA/amplifier
  - −3 dB bandwidth of 16 MHz, G = +1
  - 350 ns settling time to 0.01% (2 V step)
  - Slew rate of 22 V/µs
- Good dc performance
  - 800 µV maximum input offset voltage
  - 2 µV/°C offset voltage drift
  - 25 pA maximum input bias current
- Low distortion: −108 dBc worst harmonic @ 20 kHz
- Low noise: 16 nV/√Hz @ 10 kHz
- No phase inversion with inputs to the supply rails

APPLICATIONS

- Battery-powered precision instrumentation
- Photodiode preamps
- Active filters
- 12-bit to 16-bit data acquisition systems
- Medical instrumentation

GENERAL DESCRIPTION

The AD823 is a dual precision, 16 MHz, JFET input op amp that can operate from a single supply of 3.0 V to 36 V or from dual supplies of ±1.5 V to ±18 V. It has true single-supply capability with an input voltage range extending below ground in single-supply mode. Output voltage swing extends to within 50 mV of each rail for $I_{OUT} \leq 100$ µA, providing outstanding output dynamic range.

An offset voltage of 800 µV maximum, an offset voltage drift of 2 µV/°C, input bias currents below 25 pA, and low input voltage noise provide dc precision with source impedances up to a Gigaohm. It provides 16 MHz, −3 dB bandwidth, −108 dB THD @ 20 kHz, and a 22 V/µs slew rate with a low supply current of 2.6 mA per amplifier. The AD823 drives up to 500 pF of direct capacitive load as a follower and provides an output current of 15 mA, 0.5 V from the supply rails. This allows the amplifier to handle a wide range of load conditions.

CONNECTION DIAGRAM

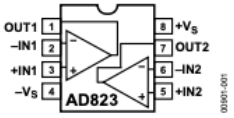

Figure 1. 8-Lead PDIP and SOIC

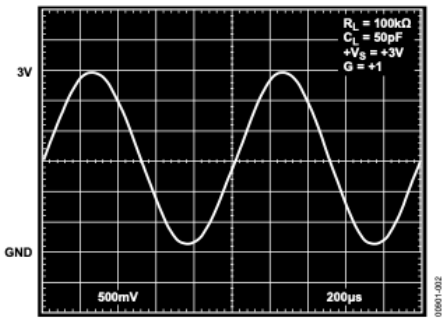

Figure 2. Output Swing, $+V_S$ = +3 V, G = +1

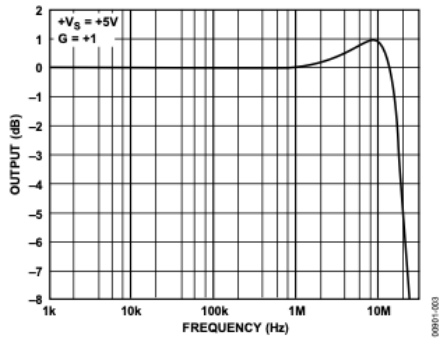

Figure 3. Small Signal Bandwidth, G = +1

This combination of ac and dc performance, plus the outstanding load drive capability, results in an exceptionally versatile amplifier for applications such as A/D drivers, high speed active filters, and other low voltage, high dynamic range systems.

The AD823 is available over the industrial temperature range of −40°C to +85°C and is offered in both 8-lead PDIP and 8-lead SOIC packages.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

At T_A = 25°C, $+V_S$ = +3.3 V, R_L = 2 kΩ to 1.65 V, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth, V_O ≤ 0.2 V p-p	G = +1	12	15		MHz
Full Power Response	V_O = 2 V p-p		3.2		MHz
Slew Rate	G = −1, V_O = 2 V Step	13	20		V/µs
Settling Time					
to 0.1%	G = −1, V_O = 2 V Step		250		ns
to 0.01%	G = −1, V_O = 2 V Step		300		ns
NOISE/DISTORTION PERFORMANCE					
Input Voltage Noise	f = 10 kHz		16		nV/√Hz
Input Current Noise	f = 1 kHz		1		fA/√Hz
Harmonic Distortion	R_L = 100 Ω, V_O = 2 V p-p, f = 20 kHz		−93		dBc
Crosstalk					
f = 1 kHz	R_L = 5 kΩ		−105		dB
f = 1 MHz	R_L = 5 kΩ		−63		dB
DC PERFORMANCE					
Initial Offset			0.2	1.5	mV
Maximum Offset Over temperature			0.5	2.5	mV
Offset Drift			2		µV/°C
Input Bias Current	V_{CM} = 0 V to 2 V		3	25	pA
at T_{MAX}	V_{CM} = 0 V to 2 V		0.5	5	nA
Input Offset Current			2	20	pA
at T_{MAX}			0.5		nA
Open-Loop Gain	V_O = 0.2 V to 2 V, R_L = 2 kΩ	15	30		V/mV
T_{MIN} to T_{MAX}		12			V/mV
INPUT CHARACTERISTICS					
Input Common-Mode Voltage Range		−0.2 to +1	−0.2 to +1.8		V
Input Resistance			10^{13}		Ω
Input Capacitance			1.8		pF
Common-Mode Rejection Ratio	V_{CM} = 0 V to 1 V	54	70		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing					
I_L = ±100 µA			0.025 to 3.275		V
I_L = ±2 mA			0.08 to 3.22		V
I_L = ±10 mA			0.25 to 3.05		V
Output Current	V_{OUT} = 0.5 V to 2.5 V		15		mA
Short-Circuit Current	Sourcing to 1.5 V		40		mA
	Sinking to 1.5 V		30		mA
Capacitive Load Drive	G = +1		500		pF
POWER SUPPLY					
Operating Range		3		36	V
Quiescent Current	T_{MIN} to T_{MAX}, total		5.0	5.7	mA
Power Supply Rejection Ratio	V_S = 3.3 V to 15 V, T_{MIN} to T_{MAX}	70	80		dB

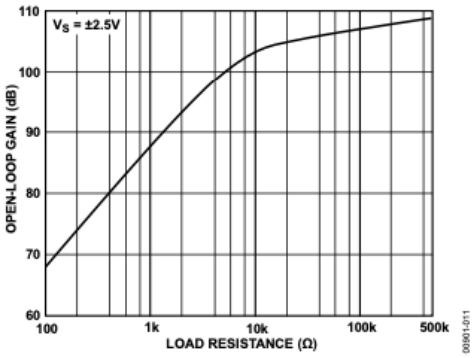

Figure 11. Open-Loop Gain vs. Load Resistance

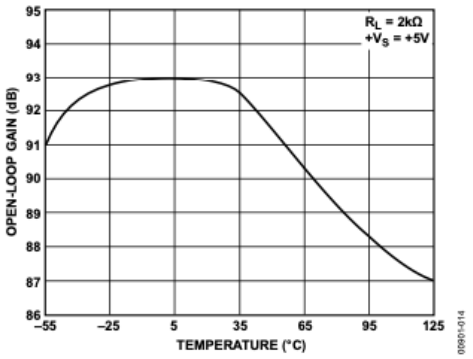

Figure 14. Open-Loop Gain vs. Temperature

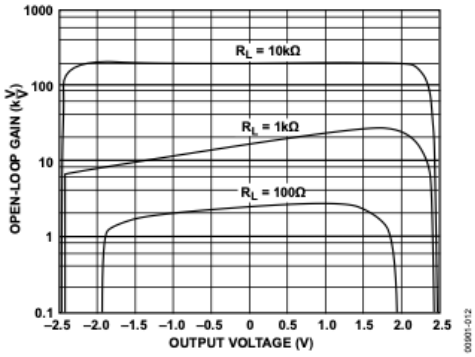

Figure 12. Open-Loop Gain vs. Output Voltage, V_S = ±2.5 V

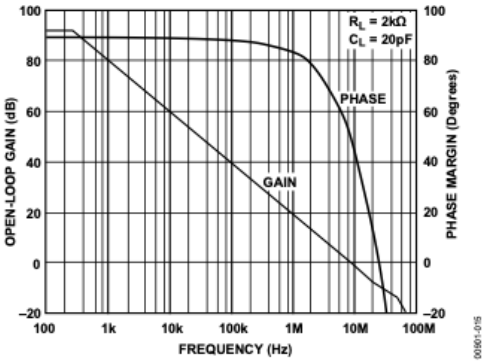

Figure 15. Open-Loop Gain and Phase Margin vs. Frequency

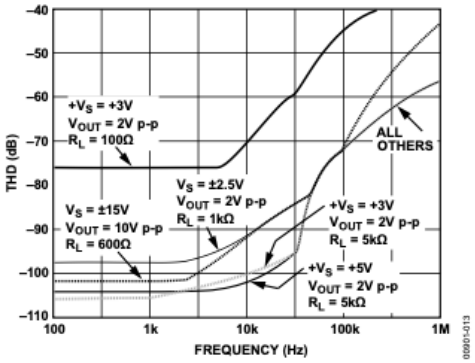

Figure 13. Total Harmonic Distortion vs. Frequency

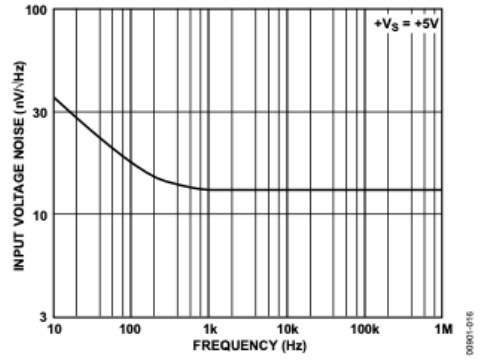

Figure 16. Input Voltage Noise vs. Frequency